Application of 3-D Transmission Electron Microscopy in Semiconductor Device Analysis

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Introduction

As features in semiconductor devices rapidly shrink to tens of nanometer size, transmission electron microscopy (TEM) has become an essential technique for process monitoring and failure analysis due to its high resolution and analytical capabilities.

Based on the sample type, TEM imaging can be classified into cross-sectional TEM (XTEM) and plane-view TEM (PTEM). The advantage of XTEM is that it shows stacked layer structures that reflect the manufacturing process steps. Plane-view TEM, on the other hand, is suitable for cases where either the exact defect location has not been isolated for XTEM or the anomaly has affected structures more laterally than vertically. A combination XTEM and PTEM will permit three-dimensional (3-D) characterization of the defect. A 3-D TEM technique has been developed for such a purpose.\[1\] Three-dimensional TEM observation denotes cross-sectional viewing of an original TEM sample that provides a two-dimensional (2-D) image. The original TEM sample can be either a cross section or a plane view.

3-D TEM

Three-dimensional TEM specimen preparation is performed in two steps. The first step in TEM imaging involves the creation of a thin section at the target location that is electron transparent. The second step requires a 90° rotation of a portion of the thin section relative to the original specimen orientation, so that the thin target area is facing the electron beam in the TEM along a direction 90° from the first imaging direction. The sample preparation procedures for the first step are easily performed with a focused ion beam (FIB) instrument; however, the second step can be challenging. In various publications,\[2-6\] the rotation of the thin section is accomplished by transferring the specimen to a second grid. The transfer process can be complex and result in a low yield of 3-D specimens.

A new and improved sample preparation technique was developed by Wang.\[7\] This technique uses an FIB instrument for the 90° rotation of a small portion of the specimen on the original grid by taking advantage of static force. All sample preparation steps, including thin-section creation and sample tilting, can be accomplished in a single process. The procedure is monitored in a high-resolution FIB instrument to assure a 100% success rate. Figure 1 shows a scanning electron microscope image of a 3-D TEM sample with two rotated sections. The original TEM sample is a lift-out sample laid on carbon film.

Applications of 3-D TEM

Gate Oxide Rupture

The 3-D TEM technique was originally developed

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for cases where cross-sectional viewing was desired, but no precise target had been pinpointed. A good example is localization of gate damage in a large capacitor. A PTEM was first carried out to localize the defect, followed by XTEM through the identified defect area.\[8\] Figure 2 shows the first 3-D TEM analysis, performed in 1999 at Precision TEM, of gate oxide rupture in a capacitor. Plane-view TEM was performed to locate the rupture site(s), followed by XTEM to further analyze the ruptures. In comparison to the traditional chemical etching and decoration approach, the 3-D TEM analysis provided detailed information for identifying the failure mechanism and the possible root cause.\[9\]

**Electrostatic Discharge Damage**

Figure 3 shows the 3-D TEM analysis of electrostatic discharge (ESD) damage. The PTEM image indicated that the damage occurred between two contacts that were farther apart and separated by a trench, but not between the nearest contacts. Such damage revealed the current path during the ESD event. A subsequent XTEM performed along the damage path showed it to be recrystallized silicon. In this case, PTEM not only provided a direction for XTEM but also exposed the defect features (lateral size, shape, or distribution).

**Blocked Contacts**

Typically, the thickness of TEM samples ranges between 100 and 300 nm. The use of a transmitted electron beam to image thick samples that incorporate multiple device features could result in a 2-D projection of stacked 3-D features enclosed in the sample.\[10\] In amorphous materials, features composed of higher-atomic-weight (Z) elements will block or mask the lower-Z material.\[2\] For crystalline materials, the darker contrast phases will block the lighter contrast phases.

Figure 4(a) shows an XTEM image in which the WSi$_2$ (long, black horizontal band) on top of a poly line masks other features in a thick TEM sample. Further thinning of the sample removed the WSi$_2$ and revealed a void (Fig. 4b). After sectioning and rotating the sample 90°, the 3-D view displayed more details of the defect (Fig. 4c).

To avoid the 2-D projection of stacked features in standard TEM analysis, some samples must be prepared to an extreme thinness, which risks damaging the sample. The 3-D TEM method described above has the advantage of viewing the defect from different angles (XTEM view to PTEM view) and avoids the need for an extremely thin sample in order to gain the necessary information.

**Open/Resistive Contacts**

Open/resistive contacts are a common defect found in semiconductor devices. Usually, interpretation of
such images can be complex; viewing the same contact from different angles may lead to inconclusive results due to overlaying features in one image. Figure 5 shows such an application. The TEM image of a via in Fig. 5(a) shows the contact with no apparent problems. However, contact blocking can clearly be seen in Fig. 5(b), rotated 90° from Fig. 5(a).

**Silicon Substrate Dislocation**

Silicon substrate dislocation is a common defect found on semiconductor devices. Lateral locations of the dislocations can be determined by PTEM (Fig. 6). To identify the process step causing these dislocations, it is necessary to determine the depth of the dislocations in the silicon substrate. A 3-D TEM application shows the location of the dislocations from the surface of the sample (Fig. 6).

**Summary**

Three-dimensional TEM can be used for defect analysis when:

- Precise defect locations are not available for XTEM.
- Features composed of heavier elements obscure the targeted defect.
Application of 3-D Transmission Electron Microscopy (continued)

Fig. 6 3-D TEM analysis of dislocations. (a) PTEM image of dislocations. (b) XTEM image of same dislocations

- Multiple features overlap and result in a complex TEM image.
- A different viewing angle is necessary.

The TEM sample thickness has remained constant for several years due to the physical limitation of sample preparation techniques. As device features become smaller, multiple features or layers will be included in the TEM section. It will be difficult to identify a defect in a specific layer when multiple features block the defect. The 3-D TEM will be an attractive technique for defect analysis and root-cause determination in such samples.

References


About the Authors

Nathan Wang received his M.S. degree in materials and metallurgical engineering from the Illinois Institute of Technology. He has worked in the field of semiconductor failure analysis since 1993. Nathan joined Spansion Inc. in 2006. His interest is currently focused on physical failure analysis, including FIB and TEM. He has authored or co-authored 18 papers in the field of semiconductor device analysis and holds a U.S. patent on TEM sample preparation.

Susan Li is the manager of Sunnyvale Device Analysis Lab and a Senior Member of the Technical Staff at Spansion. She is also responsible for supervising Spansion’s world-wide device analysis operations at five lab sites located in Penang and Kuala Lumpur, Malaysia; Suzhou, China; Bangkok, Thailand; and Aizu, Japan. During her 11-year tenure with AMD and 4-year tenure with Spansion, Susan worked on multiple products, including networking, wireless, microprocessor devices, and recently the flash memory devices. Her main focus is to support design teams, product lines, and manufacturing groups for analyzing customer returns, debugging new products, and performing failure analysis on existing products for quality and yield improvement. Before she joined AMD in 1992, Susan earned a Master’s degree in materials science and metallurgy from Carnegie Mellon University in 1990 and a B.S.E.E. degree in electrical engineering from Peking University, China, in 1985. She has published 19 papers at international conferences and currently holds 18 U.S. patents.