HOW TO DO FAILURE ANALYSIS FOR STRESS CRACKS

David Burgess, Accelerated Analysis
davidburgess@AcceleratedAnalysis.com

INTRODUCTION

Failure analysis is all about finding pertinent questions with meaningful answers.

How do you do failure analysis for stress cracks? This is, of course, a dumb question. The obvious simple answer is: you don’t. You don’t know stress cracks are the cause of a failure before the analysis is done.

The simple answer is correct but not helpful. Dumb questions often point to valid and real questions. In this case, a real question is: “If stress cracks were the cause of a failure, how can that conclusion be discovered and supported?” That is a good question and an important one. Chances are that the correct conclusion will be missed or delayed unless the analyst is familiar with the physics and history of stress voids in integrated circuits (ICs). Without a firm concept of mechanical stress in ICs and IC packaging, many failure mechanisms may not be recognized or appreciated until later ... maybe too much later.

New metallization systems have largely replaced the aluminum and aluminum/silicon conductors that were commonplace in the examples that follow. The stress void mechanism described remains important in today’s most advanced metal systems. In fact, stress in metallization may be more critical because of reduced dimensions and multiple metal layers. We’re engineering around the problem, but the stress is still there and may be a mechanism that can “bite” us again if we’re not vigilant.

BACKGROUND

Stress cracks, or stress voiding, in IC metallization were not a problem until 1980. Electromigration was a major focus. However, metal opens were occurring in high-temperature operating life, after temperature cycle, and after time in room-temperature storage. Opens were found immediately after wafer processing. Clearly, electromigration could not be the cause of failures after unbiased storage.

Stress cracks were found in products from manufacturers worldwide. Attempts to screen out potential failures were not successful. The failure rate due to stress voiding (or “creep”) seemed to increase with time. That is, stress voiding was a wearout mechanism that started at time zero.

BASIC CAUSE OF STRESS CRACKS

Aluminum has a coefficient of thermal expansion (CTE) of $26 \times 10^{-6}/^\circ C$. The CTEs of $SiO_2$ and silicon are approximately $0.5 \times 10^{-6}/^\circ C$ and $3.5 \times 10^{-6}/^\circ C$, respectively. Deposited aluminum adheres well to $SiO_2$. Good adherence to $SiO_2$ is necessary for IC manufacture, but adherence results in mechanical stress in a deposited aluminum film. Aluminum was deposited at elevated temperatures near $300 \, ^\circ C$. When cooled to room temperature, aluminum tended to shrink approximately 50 times more than its $SiO_2$ substrate. An unavoidable tensile stress is left in the aluminum close to the $SiO_2$. The oxide stretches the aluminum. The mechanical force tends to pull the aluminum apart. Note that while the aluminum is in tension, the substrate oxide is in compression.

After metal deposition, the metal is patterned and subsequently covered with a passivation layer, with the wafer heated to approximately $400 \, ^\circ C$ for passivation deposition. As applied, the passivation layer is in compression. Aluminum lines become highly stressed by nitride and oxide that encapsulate and restrict the metal on top, bottom, and both sides. All of this creates more tensile stress in the aluminum.

Although aluminum is a rather soft metal, it is also brittle. Under tensile stress, a brittle material does not stretch and elongate. Deposition variables such as the addition of silicon or nitrogen can make the film more brittle. Stress voiding is made more severe for more brittle metal.

Similarly, passivation films tend to be compressive. Passivation material and deposition details are as important to stress voiding as the metal itself.
OBSERVATION OF ALUMINUM STRESS CRACKS

Very small cracks in aluminum are not detectable by optical or scanning electron microscopy while the passivation is intact. Figures 1 and 2 show typical aluminum lines after passivation removal. Figure 1 is an optical photo showing wedgelike voids at the metal edge. Wedgelike voids do not cause failure, but they are characteristic of stress voiding. Material that was previously in the void has been pulled into the remaining aluminum on either side. Stress in the aluminum is therefore lessened. Figure 2 shows a cracklike void totally across a metal line. Obviously, such cracks cause the line to be electrically open. Cracks may occur most frequently at oxide steps, where stress is enhanced. Cracks may also be where the strength of a line is compromised by a material weakness such as a silicon nodule. Such precipitates effectively reduce the cross section of aluminum, therefore reducing its strength. However, cracks can occur anywhere along a line.\textsuperscript{[5]}

SUMMARY OF STRESS VOID SYMPTOMS

Stress voiding is most prevalent in aluminum lines less than 3 µm wide. Voids may be coincident with silicon nodules or oxide steps. However, voids can occur anywhere without discontinuities that concentrate stress or weaken line strength. Longer lines also tend to be more susceptible to stress voiding, but this is not a necessary condition.

Void failures may occur immediately after fabrication and continue to occur with time. Failure rates may increase with moderate temperature increase. However, failure rate decreases for very high temperature, because the driving tensile stress is relieved as metal temperature approaches deposition temperature. Note that this is a countercondition to most other reliability mechanisms where heating is used as an accelerating factor. Failures are also found in high-temperature operating life, but nominal current and voltage conditions are not a factor.

Although aluminum is a soft metal, it is also a brittle metal. Additives to aluminum such as silicon and nitrogen make aluminum films harder and more brittle. Severity of stress voiding is increased for the more brittle, less ductile metal.

Passivation is as important as the metal itself in the stress void mechanism. Greater compressive stress in the passivation increases the severity of stress voiding. Silicon nitride passivation is harder than phosphorus-doped glass and therefore creates more stress in underlying aluminum.

FAILURE ANALYSIS

For the open failures described, defect sites were electrically isolated. Cracks associated with failure became

“SILICON NITRIDE PASSIVATION IS HARDER THAN PHOSPHORUS-DOPED GLASS AND THEREFORE CREATES MORE STRESS IN UNDERLYING ALUMINUM.”
visible after passivation removal. Even though the defects were clearly visible, their cause, extent, and implications were unknown. Extensive study over several years was required to understand the physics of stress-induced voiding. Because of quantum mechanical tunneling, lines with stress voiding may operate even at low frequencies. However, the voids become wider very slowly with time and eventually cause low-frequency failure. Heating and cooling can alter the failure signature and make it harder to identify. Removal of the passivation or other encapsulating layers will change stress cracks, usually making them worse. The analyst then must answer the question of whether the identified defects were present before deprocessing or are a result of deprocessing.

Today, it is understood that different CTEs of metal and surrounding oxide produce stress that induces voiding. Stress voids are a fact that must be expected. Barrier metals have been added to provide a redundant path around a void in a long metal strip. A void in a long metal strip no longer causes an electrical failure. Stress void failures are not that easily eliminated. Vias, or connections between layers of conductors, are locations where a stress void can produce an electrical open. For aluminum systems, tungsten plugs can create stress and introduce open possibilities. For copper systems, vias again offer unique possibilities of failure. Redundant vias may be used to avoid IC failure despite possible voiding. However, redundant vias may not always be possible.

In today’s ICs, many new diagnostic techniques may be required to electrically define a defect site. If the defect is in the metallization, stress cracks become a consideration. There will not be one dramatic finding that proves stress voiding as the cause. If the defect is a stress void, it will not be the only one; other voids will exist in different or similar places. Metal purity may be an issue. The analyst will be challenged to find and answer good questions that hone in on the cause. When peripheral symptoms are verified and other mechanisms have been eliminated, stress voiding will top the list. It will be up to the analyst or responsible colleagues to finalize the conclusion. The procedure may not be that different from 1980, which may be why failure analysis is still so much fun.

REFERENCES

ABOUT THE AUTHOR
David Burgess is a failure analyst and reliability engineer. He developed techniques and taught in those areas at Fairchild Semiconductor and Hewlett-Packard. He is the founder of Accelerated Analysis, a manufacturer and distributor of specialty failure analysis tools. David is the co-author of Wafer Failure Analysis for Yield Enhancement. A graduate of Rensselaer Polytechnic Institute and San Jose State University, he is a member of EDFAS and has served on various ISTFA committees. David is a Senior Life Member of IEEE and was General Chairman of the 1983 International Reliability Physics Symposium (IRPS).
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