

Purpose: To provide a technical condensation of information of interest to electronic device failure analysis technicians, engineers, and managers.

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Electronic Device Failure Analysis™ (ISSN 1537-0755) is published quarterly by ASM International®, 9639 Kinsman Road, Materials Park, OH 44073; tel: 877/983-3327; website: edfas.org. Copyright© 2014 by ASM International. Receive Electronic Device Failure Analysis as part of your EDFAS membership of \$88 U.S. per year. Non-member subscription rate is \$122 U.S. per year.

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Electronic Device Failure Analysis is indexed or abstracted by Compendex, EBSCO, Gale, and ProQuest.

ELECTRONIC DEVICE FAILURE ANALYSIS™

a resource for technical information and industry developments

NOVEMBER 2014

VOLUME 16, ISSUE 4

Articles

4 Failure Analysis: Why Mistakes Are Made and How to Avoid Making One

David Burgess

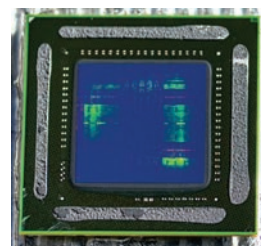
Falsely identifying an incorrect cause is the biggest failure analysis mistake possible. Learn how to recognize common FA mistakes and how to avoid them.



14 Contoured Device Sample Preparation for ±5 μm Remaining Silicon Thickness (RST) Tolerances

Chris Richardson

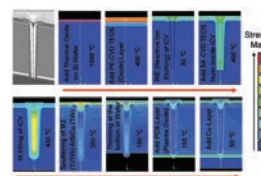
This paper describes a methodology for preparing contoured devices by using a milling machine in conjunction with a spectral reflectance measurement system for meeting ±5 μm RST tolerances.



20 3-D ICs: Progress Updates, Reliability Concerns, and Failure Mechanisms

Timothy Lenihan, E. Jan Vardaman, Greg Caswell, and Craig Hillman

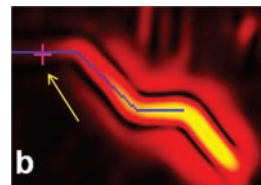
The industry has seen much progress in the development of 3-D ICs with TSVs. Read about the remaining challenges for high-volume manufacturing, reliability, and assembly.



26 Magnetic Current Imaging Revisited

Dave Vallett

This article reviews MCI basics and offers a new discussion on its capabilities, including an example of backside submicron die-level localization.



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About the Cover

See page 24 for a description of the contest winners' collage on the cover.

Author Guidelines

Author Guidelines are available at <http://www.edfas.org>.

3-D ICs

3-D TSV trends. Jan is a member of the IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society, International Microelectronics and Packaging Society, Institute for Interconnecting and Packaging Electronic Circuits, Microelectronics Packaging and Test Engineering Council, and Semiconductor Equipment and Materials International. She was elected to two terms on the IEEE CPMT Board of Governors. Prior to founding TechSearch International, Jan served on the corporate staff of Microelectronics and Computer Technology Corporation, the electronics industry's first precompetitive research consortium.



Greg Caswell, a Senior Member of the Technical Staff for DfR Solutions, is an industry-renowned expert in the fields of surface-mount technology, advanced packaging, printed board fabrication, circuit card assembly, and bonding solutions using nanotechnology. He has been well regarded as a leader in the electronics contract manufacturing and component packaging industries for the past 30 years. Prior to joining DfR, Greg was the Vice President of Engineering at Reactive Nanotechnology (RNT), where he led application development for the RNT Nanofoil and ensured a successful transition of product technology to Indium Corporation. His previous appointments include Vice President of Business Development for Newport Enterprises, Director of Engineering for VirTex Assembly Services, and Technical Director at Silicon Hills Design. Greg holds a B.A. degree in management from St. Edwards University and a B.S. in electrical engineering from Rutgers University.

Craig Hillman is the Chief Executive Officer and Managing Partner of DfR Solutions. His specialties include best practices in design for reliability, lead-free transitioning strategies, supplier qualification (commodity and engineered products), passive component technology (capacitors, resistors, etc.), and printed board failure mechanisms. Dr. Hillman has over 40 publications and has presented on a wide variety of reliability issues to over 250 companies and organizations. He received a B.S. in metallurgical engineering and materials science from Carnegie Mellon, a Ph.D. in materials from the University of California, Santa Barbara, and held a postdoctoral fellowship at Cambridge University.



About the Cover

- 1 Blossoming tulip. A 3-D visualization on a secondary emission from LADA in DDR memory circuitry of a failed unit. This abnormal emission was present from the continuous test looping of the failing structure. *Photo by May Ling Oh and Kian Fei Lee, Intel Corporation, Third Place Winner, False Color Images.*
- 2 Optical image showing adhesion issue between die-attach material and backside of the silicon die. The image was obtained after mechanical removal of the die flag with the help of laser ablation of the surrounding epoxy mold compound. The delamination pattern is quite psychedelic! *Photo by Thomas Zirilli, Freescale Semiconductor, Second Place Winner, Color Images.*
- 3 Baby seal peeking through the ice. Gate-source gate oxide rupture on 250 nm technology deprocessed from the backside. *Photo by Eric Cattey, Freescale Semiconductor, Second Place Winner, Black & White Images.*
- 4 Blown-out via. High current passed through the circuit, which led to the via blowup. *Photo by Hemachandar Tanukonda Devarajulu, Intel Corporation, Third Place Winner, Color Images.*
- 5 SEM tilt-view image of a solder ball after applying a tin etch. Shading in the image was obtained by using a negative-biased Everhart-Thornley detector and a high beam current. *Photo by Alain Gauthier and Sherri Griffin, Chipworks, Third Place Winner, Black & White Images.*
- 6 A diffusion barrier defect between tin bonding material (red) and a GaN-based LED (cyan) was found with LIVA and mapped with TEM/EDS. Tin diffused along the pinched edges of tungsten (green) and platinum (blue) layers to react with and thicken the platinum, causing nonuniform current injection and reliability concerns. *Photo by Mary A. Miller, Sandia National Laboratories, Second Place Winner, False Color Images.*

All images from the 2013 EDFAS Photo Contest.