Yield enhancement using a combination of wafer level Failure Analysis and defect isolation software: case studies

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Abstract
Yield enhancement has always been an important topic but even more when processes are moving towards smaller geometries. Today, latest FA flow intends to check wafer quality to monitor production in real-time. The purpose is to adjust any derivation coming from the process as fast as possible. The Atmel-CIMPACA laboratory located in Rousset, France, can do Failure Analysis on wafer, thanks to its wafer prober designed to work on DCG systems equipment and integrated CAD software (Meridian, Emiscope, NEXS software suite).

Wafer level yield analysis typically requires long setup and multiple dies analysis. Each of the die can be studied with a set a failure analysis (FA) techniques (photo or thermal) emission microscopy [1], laser stimulation techniques [2] or even dynamic probing using time resolved emission [3],[4] or laser based techniques, for the most common ones [5].

Introduction
This publication aims at showing how EMMI (photo emission) and OBIRCH (thermal laser stimulation technique using the 1340nm laser) analyses can be improved by software tools like a layout viewer with net tracing capability and CAD overlay. The methodology, introduced in the next three case studies, proves that the major failure mode can be known quickly thanks to this combination technique and can be located accurately before the physical analysis.

These case studies were related to final products. The electrical wafer sort (EWS) has shown a loss of yield, and some wafers were selected for the following analyses. The technology features are 0.18um CMOS gate width 0.18um on 200 mm silicon wafers. The silicon wafer substrate is always thinned to 150um after CMP (chemical and mechanical polishing) for better backside acquisitions.

Example 1:
In this first one, we studied 7 dies on the wafer that were reported as being defective after an Iddq test. We use a D10 tester supplied by Credence to apply the right electrical setup on the chip. This one requires 241 I/O pins and a test pattern larger than 15000 vectors. After the preconditioning pattern execution, the consumption on the logical and memories power supply falls from about one 1mA to less than 4µA on a good die. The yield loss is seen on several dies when the standby current is 11 µA, corresponding to an over consumption of about 7 µA between good dies and bad dies (see Figure 1 and Figure 2).
This electrical setup is critical to configure the chip in a good state. Indeed if the pattern does not pass, a lot of EMMI points can be observed, mainly in the analog part and a few points can be seen in the logical area, even on a good die. These spots disappear as soon as the pattern is fully applied. So we can focus on the EMMI points seen after applying the pattern. Some of these ones appear only after executing this pattern, and the defect can be seen only when the chip is well configured (see Figure 3).

7 dies showed emission which was observed from low magnification (0.8x) to high magnification (100x). The CAD was overlaid as shown on Figure 3 and Figure 4 at the highest magnification.

We concentrated our analysis on the EMMI points because we supposed that the EMMI points were due to a gate voltage applied on the transistor. This voltage was not the expected one due to the physical defect. So we superimposed the layout and the EMMI pictures in order to know exactly which nets were not well polarized –(Figure 3 left picture)-. A net tracer in the layout viewer enabled us to know exactly which nets were implicated in the polarization of the light emissive transistors –(Figure 5), EMMI point are on blue circles- and to highlight these nets. On 6 out of 7 analyzed dies, we could see that all the emissive cells were connected to two nets and the net trace showed that these 2 nets were much closer to each other at M4. So we focused the physical analysis between these 2 nets on M4 - red circle-.
We suspected a Barrier M4 bridging that was confirmed by physical analysis as shown on Figure 6.

The highlighted net trace in Figure 8-right allows a better picture of the link between emissive spots that are joined along the same net; all these cells are far from the drain which forces the voltage on this strip. On the contrary, we notice that all the transistors driven by this net and close to the drain supplying the voltage do not emit light. So we suspect a defect in net metallic strip between the last non emitting light transistor and the first emitting light transistor. The layout shows that 2 stacked vias metal 1 to metal 2 and a M2 strip can cause such EMMI. Next step is then to focus the physical analysis on this small area.

A charge contrast on M2 demonstrated that one of the 2 suspected vias was opened – Figure 9 left picture- so the defect was localized under metal 2. A TEM plan view allowed a view of a slurry defect – Figure 10.-, the silicon interface between the via 1 and the metal 2 prevented the current to go through this structure.

Example 2:

In the second example, the yield loss was also due to an over consumption – 20µA-. The electrical setup was easier to perform. 5 parts were analyzed on the wafer. On each part, we could see a lot of EMMI spots – Figure 7.- The analysis of these points was more difficult, and we did not have any clue of the physical defect based solely on the picture. These transistors could be identified with a layout overlay and so we traced the net connected to each gate. They happened to share a common net as shown in Figure 8.
Example 3:

In the third example, the yield loss was also due to an over consumption – 120µA-. Only 4 probes were needed to perform the right electrical setup. 5 parts were analyzed. On each part, we had an EMMI and OBIRCH signature (Figure 11). As expected there was a delocalization between OBIRCH and EMMI, several points of OBIRCH and EMMI have been highlighted. So as before, we tried to link all these points.

With a higher magnification (100x), we succeeded to identify each EMMI and OBIRCH points. - Figure 12-

The net trace succeeded to link all EMMI points to 3 nets. The 3 OBIRCH points corresponded to the drain of these nets. We noticed that the shape of the 4th OBIRCH spot was different (see elongated spot on Figure 12) and we suspected that it was the location of the defect itself. The 3 highlighted nets were closed to each other at M3 (Figure 13). So we suspected an M3 bridging on the 4th OBIRCH spot.

The physical analysis confirmed the defect location on the 4th OBIRCH spot. We recorded the defect after a top view inspection on M3 and a cross section had showed clearly a puddle on metal 3, the bridging looked like a W short just under this metallization (Figure 14).
Conclusion:

In conclusion, we have shown that the integration of the software non only speeds up the analysis but in some cases is enabling the FA engineer to know the type of defect before doing the physical analysis. We have also shown that in some cases we would not have been able to succeed in our task without using this FA software package; this is the case in example 1 and 2. So we increase the rate of success of our failure analysis and although we spend more time to perform the localization and the electrical analysis, the physical analysis goes faster. New kinds of defects which are very difficult to find or can not be found in an Idd analysis, will be found more easily.

Actually, this methodology of FA is always used in our laboratory on silicon wafer products, and helps us to improve our performance in production area by monitoring our yield constantly.

References


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