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Purpose: To provide a technical condensation of information of interest to electronic device failure analysis technicians, engineers, and managers.

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Szu Huat Goh, Boon Lian Yeoh, Guo Feng You, and Jeffrey Lam

Optimization of FA resources is critical in today's accelerated product time-to-market, especially as the cost of FA increases. This article examines a wafer-level method of FA prioritization to achieve standard production workflow.

14 Electromigration History and Failure Analysis

David Burgess

Electromigration is an important cause of IC failure; however, it is difficult to recognize and prove. Read about the history of electromigration as well as observations and checklists to help determine this wearout mechanism as the cause of failure.

20 Focused Ion Beam (FIB) Circuit Edit

Taqi Mohiuddin

With the rising cost of bringing a device to market, manufacturers seek ways to improve design success while saving time and money. FIB circuit edit is a valuable tool for reducing costs, improving design performance and functionality, and cutting design time.

26 Cleaving Breakthrough: A New Method Removes Old Limitations

Efrat Moyal and Ekkehart Brandstädt

The scribe-and-cleave method is a widely used sample-prep technique; however, numerous challenges make it less than ideal. A new indent-and-cleave approach provides improved results, even on samples previously perceived as "noncleavable."

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About the Cover

Image showing a clock net on an NVIDIA 28 nm graphics processing unit chip that was illuminated using electron beam absorbed current (EBAC) performed on the backside of the device. The bulk silicon and source/drain diffusions have been removed to enable the nanoprobe to land directly on the silicide source/drain regions. This EBAC/SEM composite image was taken with a DCG Systems nProber with accelerating voltage set to 10 kV. Photo by Robert H. Newton, DCG Systems, and Jane Li, NVIDIA. First Place Winner in False Color Images, 2013 EDFAS Photo Contest.

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