Semiconductor integration and failure-detection methods have made huge progress in the last 40 years. Every conference deals with new methods to localize failures in nanostructures, tricky case studies, and adventurous preparation techniques for devices and packages that, 10 years ago, would have subjected one to psychological examination due to an overflow of phantasy. Respect is due to everyone who contributed to this success story!

However, upon reflection, aren’t we in a labyrinth with a dead end? Is it really of interest to localize a hidden open within a submicron device by using a $1 million setup that combines, for example, magnetic microscopy and time-domain reflectometry? Hmm... yes and no. Those of us who deal with semiconductor process control or process failure analysis certainly will benefit. But what about those who deal with root-cause findings? Frankly, when considering the customer’s expectations, I have some doubts.

Moore’s law didn’t pass by without affecting other electronic components, such as capacitors, hybrid relays, and so on. Electronics became much, much more complex and powerful. Comparing the electronics of a car from the 1980s with one from today and, concurrently, comparing the related failure statistics tells us that we must not neglect the system aspect. Hand on heart: How often did you conclude an analysis with “electrostatic discharge/electrical overstress” recently? In most cases, it’s just an academic circumscripti9on that the device suffered severe destruction, but nothing conclusive was found as the root cause. If 8D reports frequently abound with “Not Applicable” in many columns, something must be wrong with this procedure. Are we asking the wrong questions? Is it really of importance that the MOSFET located in the output driver at position $X - 342X = 677$ suffers from a pinhole gate leakage, or would it be enough to know that output $X4$ is leaky?

Again, two worlds of thinking meet at this point. The process controller may need the pinhole information. But what about the service manager of the failed industrial control electronics? He will ask other questions: “Why did this component fail?” If it happened several times with the same component from different lots, he will question whether the problem is PCB circuitry or system related. Is it an inductance that responds with transient spikes to a signal change? A long wiring on the PCB or by cable that catches electromagnetic interference? A capacitor that falsifies signal pulses? Environmental conditions that borderline the specifications? Periodical, short-time electrical overstress? Hot plugging? Many more questions arise when reflecting on the electrical and environmental ambience of the application. By the way, this process is called anamnesis, meaning “prior to analysis.”

In the end, only two questions are of interest to our clients: “What can be done to avoid the failure in the future?” and “How can potentially affected devices/PCBs or systems be sorted out (by useful testing)?” The ability to answer even one of these two key questions requires a sound understanding of the root cause. If, however, the root cause is not device related, then using only device analysis will not meet the expectations of the client.

Failure analysis is more than just semiconductor analysis. It also includes passive components, PCBs, wiring, and so on. We need to understand not only components but also systems and applications. And, we need the courage to confront our customers in the supply chain with this certainty. “Solving the problem together” must become the paradigm of the future, instead of fearing the loss of our customer’s confidence when we ask awkward questions.

The ISTFA 2014 Panel Discussion will focus on the topic “System-to-Component-Level FA in the Space and Oil Industries.” Let’s extend our horizon beyond the scope of semiconductor devices. Feel encouraged to share your passive components and system-level failure analyses with our community. Let’s learn and think together, keeping the system in mind!

I look forward to seeing you at ISTFA.

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Letters to the Editor: EDFA encourages your participation. Send your comments and suggestions to Felix Beaudoin, EDFA Editor, at felix.beaudoin@globalfoundries.com.
WHEN FA = FAST ANSWERS

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Backscatter electron image of cross section of wire bond.

EBSD (Electron Backscatter Diffraction Analysis) image of wire bond cross section.

EBIC (Electron Beam Induced Current) image of electronic device.

S/TEM EDS map of integrated circuit cross section.

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