Yield-Oriented Logic Failure Characterization for FA Prioritization

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Introduction

Although technological developments have changed the semiconductor scene dramatically over the past years, one thing that has not changed is the competitive nature of the industry. Companies are constantly exploring ways to accelerate product time-to-market and reduce manufacturing cost. With the rising cost of failure analysis (FA) and with FA being a significant stakeholder in the manufacturing value chain, FA resource optimization is necessary. One way to achieve this is prioritization.

Prioritization is a standard practice in software fault isolation (FI) tools such as static random access memory (SRAM) bitmapping and electronic device automation-based logic scan diagnosis. In SRAM bitmapping, physical representations of fail bits are classified into different signatures, such as single bits, pair bits, or a four-bit cluster, to create a Pareto chart that guides FA candidate selection.[1] Priority for FA is assigned to the candidates with the highest yield impact to enable maximum learning.

For logic, design-for-test (DFT) structural elements, such as flops and latches, are usually implemented in the design to enhance testability and observability for faults.[2] Scan diagnosis interprets the mismatch behavior of the combinational logic circuits against expected responses after structural testing to predict failure suspects.[3] In addition to confidence score and suspected fail path length, a second step, known as volume statistical analysis, searches for systematics and assesses the potential yield impact for FA prioritization. Some examples of common analytical methods include fail net stacking and suspect fingerprinting based on net identities or cell names.[4] Figures 1(a) and (b) depict the workflows for SRAM bitmapping and scan diagnosis, respectively.

Although it is proven in industry that a yield-oriented prioritization approach established on software-based FI is effective to identify critical candidates to enable a fast yield ramp, it is not well internalized into typical hardware-based FI workflows.
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Generally, logic in an IC can be categorized into analog and digital. For analog logic and digital logic that is not within the fault coverage of DFT structural test and diagnosis, it is well known that static FI techniques are not effective unless the fallout is caused by gross process defects, power-related failures, or high leakages. Therefore, tester-based FI is often the go-to solution. Conventionally, most tester-based FI is performed through the silicon backside on packaged parts, adopting a workflow as shown in Fig. 2. Whenever a functional failure is revealed on sort test, failing dice are packaged soon after to avoid delay in debug turnaround time. These failing dice are usually selected from a specific wafer with signature or failure modes (hard or soft fails) of interest.

Under the current workflow, there are no prior insights into the electrical failure signatures for the entire population of failing dice. There is a lack of statistics for detailed assessment on potential yield impact to prioritize FA activities. This article describes a yield-driven approach to characterize IC logic failures at the wafer level. The principal objective of this step is to classify the failing dice according to their failure responses on ATE to relevant test vectors and external stimuli. Every failure category is anticipated to be possibly caused by a different failure mechanism. The entire wafer is characterized to ensure there is sufficient statistical data to estimate the potential yield impact of each failure category to determine the priority for debug. The next section describes, using real test cases, some methods for failure characterization.

**Results**

**Characterization on Dynamic Current**

A case of functional failure on an IEEE 1149.1 controller, also commonly known as JTAG (Joint Test Assembly Group), is discussed. The $V_{DD}$ digital power supply dynamic current is monitored at each test cycle of the JTAG test pattern for every failing die. The characterization results are presented in Fig. 4. Figure 4(a) shows the dynamic current from good dice that pass JTAG. Obvious modulations are observed between 7500 and 12,500 test cycles. Figures 4(b) and (c) illustrate the characteristics of the bad dice, whose current modulates similarly to the reference dice, and those whose current does not modulate at all, respectively. The population of bad dice can be categorized into two main groups according to Fig. 4(b) and (c), labeled as classification 1 and 2, respectively. The yield loss is calculated and the results are shown in Fig. 4(d). Because classification 1 dice contribute a significant 90% of the yield loss, it is obvious that they should be investigated as the first priority.

**Yield-Oriented Prioritization for Product Logic FA**

The proposed workflow is depicted in Fig. 3. In comparison to Fig. 2, the distinct difference is the addition of failure characterization followed by prioritization after the failure is verified on the automated test equipment (ATE). The principal object of this step is to classify the failing dice according to their failure responses on ATE to relevant test vectors and external stimuli. Every failure category is anticipated to be possibly caused by a different failure mechanism. The entire wafer is characterized to ensure there is sufficient statistical data to estimate the potential yield impact of each failure category to determine the priority for debug. The next section describes, using real test cases, some methods for failure characterization.
Characterization on Test Vector Responses

A second case of a digital-to-analog convertor (DAC) voltage reference ($V_{\text{ref}}$) failure is discussed. Conventionally, such failing dice are treated equally if there is no wafer signature, and they are sent for packaging in preparation for subsequent FA. In perspective, some form of characterization should be pursued on ATE before packaging. Figure 5(a) shows a measured plot of $V_{\text{ref}}$ against another DAC-related functional test. The bold lines represent the lower and upper allowable limits. Although a linear correlation is observed, two groups of $V_{\text{ref}}$ failing dice apparently exist: those that fail only $V_{\text{ref}}$ test and those that fail both functional tests. This implies the possibility that two failure mechanisms are involved. The yield impact is calculated and illustrated in Fig. 5(b). Based on this analysis, the first type of failing dice is identified to be of higher priority for debug. It was later found from dynamic photon emission microscopy that both groups of bad dice actually reveal similar emissions as compared to the reference. This indicates that any fix solution that arises from debugging on the first group of bad dice will likely resolve the issue of DAC $V_{\text{ref}}$ completely. From this example, it is evident that a detailed wafer characterization in combination with FI results has the benefit of anticipating the potential yield recovery impact more accurately. This information is valuable to product engineering.

In another case, JTAG failing dice are characterized on quiescent current ($I_{\text{DDQ}}$) and $V_{\text{DD}}$ Kelvin tests. The results on selected dice are summarized in Fig. 6(a). The $I_{\text{DDQ}}$ is measured at 25 and 85 °C. The $I_{\text{DDQ}}$ increment factor is calculated by 85/25 °C. A factor of

![Fig. 4](Dynamic $V_{\text{DDO}}$ digital supply current of (a) good dice that pass JTAG, (b) category 1 bad dice, and (c) category 2 bad dice. (d) Yield-loss percentage Pareto chart)
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2 to 3 times indicates possible front-end-related issues. Two main categories of failing dice are identified. The first group consists of $V_{DD}$ Kelvin values less than 0.9 V and an $I_{DDQ}$ increment factor of less than 1. The second group shows no degradation in $V_{DD}$ droop and an $I_{DDQ}$ increment factor greater than 2. A more detailed whole-wafer analysis is shown by a plot of $I_{DDQ}$ with increment factors (Fig. 6b). The vertical line demarcates the two groups of failing dice. Because the first group has a higher yield impact, it will be focused on as a priority. Further characterization on dynamic photon emission confirms the presence of the two categories of failure. Unlike category 1 failing dice, an emission spot exists in control block A in the second category.

Characterization on External Stimulus and Test Modes

The last test case is a phase-locked loop failure.

The failing dice on the wafer are characterized according to temperature effects and three different test modes. The latter involves register access to either boost the start-up current or vary other test conditions. Typically, such test modes are available for engineering purposes, and their test patterns must be generated separately from production-sort test requirements. The yield impact of different test conditions is calculated from the percentage recovery of failing dice based on the entire population of fails on the wafer. The Pareto chart in Fig. 7 shows the results. It is obvious that test mode 3 should be investigated first, and those soft failing dice that respond to thermal stimulus are insignificant. This is another model example indicating that not all functional failing dice should be debugged equally based solely on the sort data outcome. Follow-on dynamic photon emission and soft defect localization, as shown by the insets in Fig. 5.
Fig. 7, confirm the existence of the different categories. The FI results also showed the possibility of reclassifying test modes 2 and 3 under the same category.

**Conclusion**

Product logic debug has always been challenging due to the lack of control and observation test points. This is especially so for foundries with limited design information. With devices becoming more complex as technology nodes advance, more FA resources are required to resolve logic failures. This trend directly affects the profit margin and will become worse with the rising cost of FA, which is a business concern. To address this, it has been demonstrated in this article that a yield-oriented prioritization approach is beneficial to determine the most favorable failing dice for FA to enable a faster yield ramp. The FA resources can also be managed more systematically, thus reducing cost. This methodology can be achieved by an enhanced workflow to incorporate failure characterization and classification on ATE prior to FI activities. Three different methods to characterize functional logic failures with supporting test cases are described to substantiate the advantages of this added step.

Lastly, it should also be emphasized that to capitalize from the discussed workflow, it is recommended to leverage on the recent maturity of the wafer-level tester-based FI diagnostic tool[7] as a means to further reduce both debug lead time and cost.

**References**


**About the Authors**

Szu Huat Goh received his B.Eng. and Ph.D. degrees in electrical and computer engineering from the National University of Singapore. His doctorate research on simulation and implementation of the aplanatic refractive solid immersion lens was awarded a conference Best Paper and was part of a team project that received the 2009 Singapore President’s Technology Award. Dr. Goh is currently with Globalfoundries, Product/Test and Yield Engineering, Singapore, where he leads a team responsible for product failure diagnostics and advanced methodologies to accelerate yield ramp. His main focus is on developing wafer-level fault isolation methods and leveraging cross-functional techniques to enhance yield learning. His work has been published in conference proceedings and in journals.
Boon Lian Yeoh graduated from the University of Technology, Malaysia, with a B.E. degree in electrical engineering. From 2006 to 2011, he worked for Intel Microelectronics, Malaysia, where he specialized in memory testing and failure analysis. He is currently employed as Principal Engineer in Globalfoundries’ Product/Test and Yield Engineering Department, Singapore, where he works on device fault isolation using a spectrum of FA tools, such as emission microscopy, OBIRCH, and dynamic laser stimulation techniques. His current research interests focus on exploring soft defect localization and laser-assisted device alteration techniques for different failure-type diagnostics in the semiconductor industry.

Guo Feng You holds a B.S. degree in physics from Fu Dan University, China; a Meng degree in electrical engineering from Nanyang Technology University, Singapore; and a Ph.D. degree in the same field from the National University of Singapore (NUS). Currently, he specializes in wafer-level tester-based failure debug in Globalfoundries’ Product/Test and Yield Engineering Department, Singapore. His experiences include dynamic fault isolation techniques, such as frequency mapping and soft failure localization. Prior to joining Globalfoundries, Dr. You worked as a research fellow at NUS.

Jeffrey Lam received his B.S. and M.S. degrees in chemical engineering from the University of California Berkeley and the University of California Davis in 1979 and 1981, respectively. He obtained a second M.S. degree in electrical engineering and computer science from the University of Santa Clara in 1986. In 2014, he received his Ph.D. from the school of mathematics and physics at Nanyang Technological University. Dr. Lam is currently a Vice President at Globalfoundries, Singapore, where he is in charge of the Product/Test and Yield Engineering Department in Technology Development. He possesses more than 20 years of experience in FA, design, product/yield engineering, and test development. Dr. Lam has 7 technical patents and more than 20 publications. He has also been the chairman of SEMICON Singapore’s Product and Test Committee since 2009.

Noteworthy Item

ESREF 2014

The 25th anniversary of the European Symposium on Reliability of Electron Devices (ESREF ’14) will take place September 30 to October 2, 2014, in Berlin, Germany. This international symposium continues to focus on recent developments and future directions in quality and reliability management of materials, devices, and circuits for micro-, nano-, and optoelectronics. In addition to classic topics such as failure analysis and general reliability aspects, the conference will focus on such emerging themes as organic semiconductors and wide-bandgap devices. Invited experts will provide numerous tutorials.

For the first time, two user-oriented workshops will be fully integrated within the frame of the conference: the European FIB User Group (EFUG) and the European Failure Analysis Network (EUFANET) meeting. As usual, a profound equipment exhibition, placed in the conference area, will be part of the event.

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