NOVEMBER 2015 | VOLUME 17 | ISSUE 4 edfas.org

ELECTRONIC DEVICE FAILURE ANALYSIS™

A RESOURCE FOR TECHNICAL INFORMATION AND INDUSTRY DEVELOPMENTS

4 Thinning and Polishing Highly Warped Die: Part II, A Discussion of the Mechanical Limitation of Flattening a Curved Die in Preparation for Die Thinning

Kirk A. Martin and Nancy Weavers

The mechanical variables of die thinning and polishing are discussed, with particular attention to the mounting processes and their effects.

14 Depositing Controlled, Matched Resistors for Circuit Edit of Analog Circuitry

Frank Zachariasse, Harry Roberts, and Peter van der Cruijsen

This paper describes a fast and reliable technique to achieve analog circuit edit validation by depositing, characterizing, and accurately connecting matched resistors.

22 Capacitors—The Helpers of Active Devices: A Failure Analyst's (Re)View

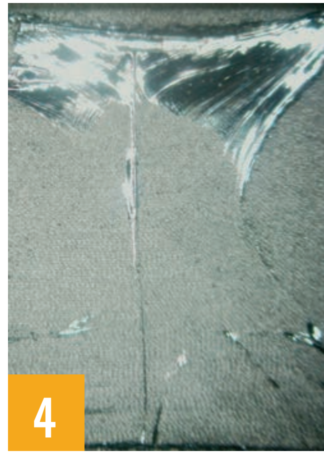
Peter Jacob

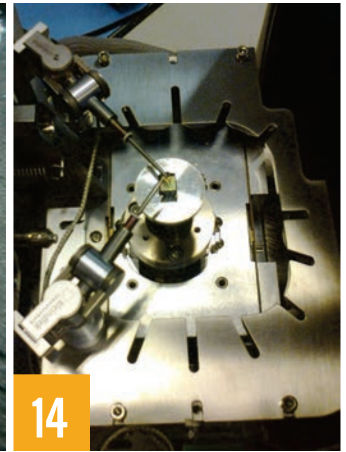
Review the frequent, but often overlooked, reliability failure mechanisms of three main capacitor groups.

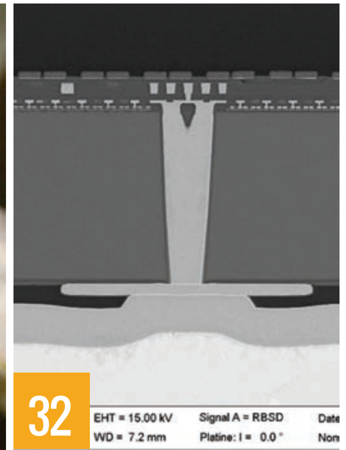
32 The Use of a Virtual Known Good Device (VKGD) to Accelerate 3-D Packaging Development

Jesse Alton, Martin Igarashi, and Ka Chung Lee

Read about a technique that can help accelerate the IC packaging product development cycle by isolating failures in the early stages.







ABOUT THE COVER

See page 36 for a description of the contest winners' collage on the cover.

Author Guidelines

Author guidelines and a sample article are available at edfas.org. Potential authors should consult the guidelines for useful information prior to manuscript preparation.

DEPARTMENTS

40 SPECIAL! ISTFA 2015 SHOW LISTING

60 ADVERTISERS' INDEX

47 ASM AWARDS

41 CALL FOR PAPERS

54 DIRECTORY OF FA PROVIDERS *Rose Ring*

56 GUEST COLUMNIST *Renee S. Parente*

2 GUEST EDITORIAL *Tom Sharpe*

52 LITERATURE REVIEW *Mike Bruce*

42 PRODUCT NEWS *Larry Wagner*

50 TRAINING CALENDAR *Rose Ring*

For the digital edition, log in to edfas.org, click on the "News/Magazines" tab, and select "EDFA Magazine."

ABOUT THE AUTHORS

Jesse Alton received an M.S. degree in physics from the University of London, Royal Holloway. He was employed at Pacific Northwest National Laboratory in Richland, Wash., where he undertook studies into the vitrification of high-level nuclear waste. He returned to the U.K. to complete a Ph.D. at the University of Cambridge, where he focused on the development of high-power terahertz sources and their applications. Upon completing his Ph.D., Dr. Alton joined TeraView Ltd. in April 2005, where he currently leads the Semiconductor Applications Group. He has authored or co-authored over 50 published papers.

Martin Igarashi has over 25 years of experience in the roles of engineering, applications engineering, sales and marketing, mergers and acquisitions, product development, and general management of product divisions in the electronic design automation, plasma etch, photolithography, test and measurement, and laser material processing industries. He has worked for companies such as Electro Scientific Industries, Toppan, ETEC Systems, Applied Materials, and Tektronix. Mr. Igarashi earned a Bachelor's degree in applied mathematics from the University of California, Santa Barbara. He currently heads TeraView's semiconductor business and is based in Portland, Ore.

Ka Chung Lee graduated with a doctorate degree in atomic laser physics from the University of Oxford in 2013. In his thesis, he demonstrated the creation of quantum entanglement between two macroscopic bulk diamonds at room temperature. Currently, Dr. Lee is a physicist at TeraView Ltd., where he researches the application of terahertz technologies as an imaging and fault-isolation tool. His main research interests lie in light-matter interactions at terahertz frequencies.

ABOUT THE COVER

a) Micromasking of wafer fab metallization defect induced at photoresist development step. A step-by-step deprocessing analysis allowed removal of the top metallization until the anomaly was clearly discerned. Consequently, a short circuit between two neighboring lines was created. The original shape looks like a dog on the lookout, with discernable nose and upright ears. *Photo by Yann Weber, Freescale Semiconducteurs SAS, Second Place Winner, Color Images.*

b) Deprocessed sample exhibiting outgassing of foreign material, causing disruption of metal circuit traces. *Photo by Jay Kopycinski, Freescale Semiconductor, Second Place Winner, Black & White Images.*

c) 3-D x-ray tomography of a 2.5-D integrated circuit showing C4 solder bumps (with solder bridging) near the bottom of the image, through-silicon vias near the middle, and microbumps at the top of the image. *Photo by Phoumra Tan, Xilinx Inc., and Allen Gu, Carl Zeiss X-Ray Microscopy, Second Place Winner, False Color Images.*

d) Electrostatic discharge damage on a protection cell after a 2.2 kV human body model stress. The part has been deprocessed down to poly level. The artifact is likened to a tree set against a setting sun. *Photo by Karl Villareal and Geert Van Huffel, ON Semiconductor, Third Place Winner, Black & White Images.*

e) Abnormal crystal growths on silicon oxide (used differential interference contrast filter). *Photo by Jin Won Koh, National Nanofab Center, Third Place Winner, Color Images.*

f) Energy-filtered transmission electron microscope image of a transistor in the 30 nm Samsung DDR3 synchronous dynamic random access memory. Elements: red = titanium, green = nitrogen, blue = oxygen. *Photo by Lina Gunawan, TechInsights, Third Place Winner, False Color Images.*

All images from the 2014 EDFAS Photo Contest.