Recently, flip-chip assembly has become mainstream for fine-pitch interconnection in large-scale integration packages. Gold studs and copper pillars with solder caps are two types of bumps in common use.\(^1\) Gold stud bumps are commonly used for interconnecting dice with peripheral layouts. Gold-gold bonding has the advantage of a low process temperature, and gold-solder with adhesive has good wettability of the joint without flux.

The use of copper pillar with a solder cap has the advantage of gang fine-pitch bumping by wafer plating. Increases in the number of bumps, narrowing of pitch, and cost pressures have driven the adoption of copper pillar/solder cap bumping in high-performance mobile devices. Copper pillar bumps on the die are interconnected to the copper pad on the substrate in a solder reflow process. The use of thermal compression bonding (TCB) and preapplied underfill for fine-pitch interconnection is growing due to its precise alignment of bump and pad and the minimization of global stress on the assembly. Concerns with the technology, however, include entrapment of adhesive components and voids in the joint due to solder shrinkage.

**FIB-SEM FOR FLIP-CHIP JOINT ANALYSIS**

Three-dimensional (3-D) analysis techniques can be used to study copper pillar bump joints. X-ray computed tomography (CT) is one major 3-D analytical method, but its spatial resolution is currently limited to the submicron level. The slice-and-view method using a focused ion beam-secondary electron microscope (FIB-SEM) has high spatial resolution on a nanometer level, which makes it superior to x-ray CT.\(^2\) This method has already been used to investigate the inner wiring of a semiconductor device. The authors used the method to evaluate the solder joint and what appeared to be preapplied underfill between a copper pillar bump and a copper trace on a substrate.

The authors removed a memory and application processor (AP) packaged in a package-on-package (PoP) from a commercial tablet personal computer (PC). First, mechanical polishing was used to expose the structure of the PoP, and then the microbump interconnecting the AP to the copper wiring on the package substrate was located. The authors then made a 3-D observation by the slice-and-view method using an FIB-SEM equipped with a dual-electron beam. An SEM image was taken every 200 nm of etching by FIB, for a total of 240 SEM images. Then, 3-D images were reconstructed using these SEM still images.

The authors also investigated the composition distribution of the solder joint area by electron probe x-ray microanalysis (EPMA). To observe thermal changes in the bumps, another sample of the PoP was subjected to a thermal cycle test (TCT) of 1000 cycles from \(-55\) to \(125\) °C with a 1 h cycle.

**COPPER PILLAR JOINT ANALYSIS RESULTS**

A cross-sectional microscopic image of the flip-chip bump interconnection of the AP die prepared by...
“THE USE OF COPPER PILLAR WITH A SOLDER CAP HAS THE ADVANTAGE OF GANG FINE-PITCH BUMPING BY WAFER PLATING. INCREASES IN THE NUMBER OF BUMPS, NARROWING OF PITCH, AND COST PRESSURES HAVE DRIVEN THE ADOPTION OF COPPER PILLAR/SOLDER CAP BUMPING IN HIGH-PERFORMANCE MOBILE DEVICES.”

Mechanical polishing is shown in Fig. 1. It seems that the copper pillar was bonded to the copper wiring on the substrate by TCB using a preapplied underfill. Figure 2 shows higher-magnification images taken by SEM. An entrapped filler particle from the preapplied underfill is visible in the solder joint area.

3-D TOMOGRAPHIC RECONSTRUCTION

Figure 3 shows 3-D reconstructed images of the joint before and after TCT. The volume of the reconstructed space of the joint before TCT is $38 \times 44 \times 47 \mu m^3$, and the volume after TCT is $44 \times 41 \times 46 \mu m^3$. Tomographic images of the XZ- and YZ-planes of the bump center are shown in Fig. 4.

The XZ-plane is parallel to the substrate plane. The X-axis is parallel to the copper trace on the substrate, and the Y-axis is perpendicular to it. The authors observed large voids, shown in Fig. 4(a) and (b) as “Voids (A).” The authors believe these were generated by solder shrinkage.[3]

The authors subjected another sample of the same package to the previously mentioned TCT and then performed 3-D SEM analysis of the solder joint. Another type of void at the interface of the copper pillar and the intermetallic compound layer is shown in Fig. 4(b) as “Voids (B).” The authors believe these were generated by solder reflow and/or mechanical stress during TCT.
intermetallic compound (IMC) was clearly visible. These are indicated as “Voids (B)” in Fig. 4(b).

ANALYSIS OF XY-PLANE SLICES

Figure 5 shows XY-plane tomographic images of the solder joints of the packages without TCT (Fig. 5a to c) and with TCT (Fig. 5d to f). The images were extracted at three different Z-heights:

- Figures 5(a) and (d), at level I (shown by arrow I in Fig. 4), are slice views of the copper pillar and IMC interface.
- Figures 5(b) and (e), at level II (shown by arrow II in Fig. 4), are slice views of the IMC layer.
- Figures 5(c) and (f), at level III (shown by arrow III in Fig. 4), are slice views at the level of the shrinkage voids.

Comparison of the two level-I views (Fig. 5a and d) shows that the copper pillar and IMC interface changed significantly with TCT treatment: although only small voids are observed prior to TCT, numerous large voids appear after TCT. At level II, very few voids were detected in the IMC layer either before or after TCT. At level III, numerous shrinkage voids and entrapped filler particles from the preapplied underfill are observed. In addition, the authors were able to observe the 3-D distribution of filler in the underfill, as well as gaps between the copper pillar and the adhesive. (continued on page 18)
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DISCUSSION OF VOID FORMATION MECHANISM

The mechanism of void formation at the interface between the copper pillar and IMC layer that occurs during TCT is discussed below.

KIRKENDALL EFFECT

The Kirkendall effect, which describes the formation of voids at the interface of different metals due to differences in the metals’ thermal diffusivity, is well known.[3,4] In a copper/tin system, as shown in Fig. 6, a Cu₃Sn IMC layer can easily grow, which creates the Kirkendall effect. The EPMA mapping results of the IMC layer in the authors’ system are shown in Fig. 7. Because there is not much growth of the Cu₃Sn layer, it does not appear that the large-volume voids shown in Fig. 5(d) were formed by the Kirkendall effect. This is supported by the fact that no such voids were observed at the interface of the substrate copper and the IMC.

GAS EXHAUST PHENOMENON AND SOLID-PHASE DIFFUSION

Studies have shown that volatile constituents inside a plated copper film can move during soldering processes, which can lead to void formation in the solder.[5]
Void formation based on this gas exhaust phenomenon is illustrated in Fig. 8. A copper pillar is formed by microplating with a certain aspect ratio, whereas the copper trace on the substrate is formed from dense electrolytic copper foil. Volatile constituents in the copper pillar are released as gas during the TCT by interface reaction with the solder.

**SUMMARY**

The authors used 3-D SEM analysis to investigate the flip-chip bump interconnection of an AP taken from a commercial tablet PC. The analysis technology is based on the repetition of FIB etching and SEM image capture. Three-dimensional views were reconstructed from 240 SEM images that were taken after repeated FIB etching at 200 nm intervals. The authors believe the interconnection to be a copper pillar with a solder cap connected to a copper trace on the substrate by thermal compression bonding with a preapplied underfill. Our analysis showed that the interconnection joint in the AP as received included filler entrapment and many voids. With this method, the generation of a number of voids was clearly observed at the interface of the pillar copper and the IMC after 1000 cycles of TCT between −55 and 125 °C.

**REFERENCES**

ABOUT THE AUTHORS

Mototaka Ito joined Toray Research Center in 1991, where he conducted analysis of semiconductors and various industrial materials using Auger electron spectroscopy. He is currently engaged in the 3-D FIB-SEM analysis of semiconductor package interconnections and the investigation of thermally induced deformation in large-scale integration packages. Dr. Ito received a master’s degree from Nagaoka University of Technology and a doctorate from Osaka University, where he studied diffusion phenomenon in the interface between SnAgX solder and electroless Au-NiP plating.

Jun Kato has been engaged in electron microscopy for over 20 years and has worked extensively in the analysis of materials in semiconductor devices and other advanced materials. Most recently, he has specialized in FIB. He is currently in charge of FIB/SEM analysis at Toray Research Center.

NOTEWORTHY NEWS

ENGINEERING EXCELLENCE AWARD WINNER

The Optical Society named the Logic Analysis Tool (LAT) team as the winner of the 2015 Paul F. Forman Team Engineering Excellence Award. The research team was formed in response to a call from the Intelligence Advanced Research Program Activity (IARPA) for innovative solutions to circuit analysis. The team developed an optics-based LAT that detects the time-resolved emission of light from switching transistors within integrated circuits (ICs) operating down to 0.5 V, thus creating a new tool for device analysis in advanced process technologies. The group, led by Dr. Euan Ramsay of DCG Systems, was comprised of the following:

- **The DCG Systems team** (Euan Ramsay, Herve Deslandes, Tom Kujawa, Ted Lundquist, and Benjamin Cain) was responsible for the construction of a system to measure the spectrum of light emitted by leaking and switching transistors so that the wavelength range of the final optical system and detectors could be defined. On the basis of these measurements, DCG also developed the optics for collecting the emitted light and bringing it to the Photon Spot fiber for time-resolved emission measurements from ICs. DCG performed the assembly and initial testing of all subsystems into one integrated tool. The final prototype configuration allowed diffraction-limited performance over a broad spectral range with a numerical aperture of more than 2.5.

- **The MIT team** (Karl Berggren, Kristen Sunter, and Faraz Najafi) designed and fabricated superconducting nanowire single-photon detectors, delivering high gain, low jitter, and low noise, for the required time-resolved measurements of the emission from switching transistors. These detectors were optimized in wavelength based on the measurements made by IBM and incorporated several novel features.

- **The Photon Spot team** (Vikas Anant, Brian Ma, and Juying Shang) developed a closed-cycle cryostat to cool the superconducting detectors to 800 mK. They also designed a low-jitter electronic interface between the fiber delivery system from the output port of the tool to the superconducting detector and the DCG Systems electronics and software.

- **The IBM team** (Peilin Song, Franco Stellari, Andrea Baghat-Shehata, Seongwon Kim, Herschel Ainspan, Christian Baks, Alan Weger, and Ulrike Kindereit) used the spectral measurement system to determine the emission spectrum trend from 45 and 32 nm process technologies at various operating voltages. IBM developed a unique test chip with features stretching the design rules for prototype characterization and performed the qualification of the various versions of the prototype tool, including on various 22 and 14 nm test chips (10 nm chips are yet to be available) using proprietary IBM test technologies. Final testing was carried out by the IBM team.
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