Laser voltage imaging (LVI) has the unique capability of mapping the periodic signal in a device under test (DUT). It is very suitable for scan chain diagnosis because data propagation through the scan chain is clocked with a periodic signal. Thus, LVI can easily identify the broken point for a scan chain failure, whether its defect is in the data path or in the clock path. Laser voltage probing (LVP) involves acquiring the waveform in a time domain from a particular point, such as the signal broken point identified by LVI, and a reference point. This can further confirm the failure and help with understanding the failure signature. This article discusses combining these two techniques in an in-line scan chain logic macro diagnosis, which has greatly improved the failure analysis success rate.

INTRODUCTION

Historically, static random access memory (SRAM) yields have been the only qualification metrics during technology development, and consequently, failure analysis of SRAM is the main feedback for process improvement and yield learning. This is because the high density and small feature size of SRAM make its yield very sensitive to process variation, and the failing bit cells can be precisely localized for physical failure analysis. As microelectronic technology progresses in the nanometer realm, logic circuits and structures are also becoming dense and sensitive to process variation. Logic failures may also have root causes different from SRAM failure. If these technology weak points for logic circuits are not detected and resolved during the technology development stage, they will greatly affect the product manufacturing yield ramp, leading to longer design time to market. Moreover, analysis of logic failure in the product is much more difficult and time-consuming, involving tester-based fault isolation and software-based scan diagnosis. Thus, it is very important to have an in-line scan chain logic macro implemented for early detection of the logic circuit weak points during technology development. Furthermore, the combination of LVI and LVP application in scan chain diagnosis has improved the in-line scan chain logic failure analysis success rate to that of SRAM failure analysis.
the silicon backside while the DUT is exercised. The laser beam reflects from the interface between the backside silicon and the active regions, such as drain and channel. The reflected laser beam has a modulated amplitude and phase. Because the modulated amplitude is dependent on the transistor state, namely the electrical field in the drain area and/or the free carrier density in the channel, extraction of the modulated amplitude of the reflected laser beam indicates the states of the transistor, on which the laser beam is focused. Figure 1 is a simplified LVP schematic. Initially, the application of LVP was mainly in design debug and device characterization, rather than fault isolation. This is because the waveforms obtained with LVP at any given time come from a particular point, namely one transistor or one node. To search for a defective transistor or node, it is necessary to probe each transistor or node one by one. It is time-consuming.

Rather than acquiring data at a single point on a DUT in the time domain, LVI \cite{7-9} collects data in the frequency domain from numerous points in the field of view on a DUT. The LVI technique rasters a laser beam across an area of a DUT through the backside silicon. At each point, the reflected laser beam is modulated in both amplitude and phase at the switching frequency of the transistor under the area on which the laser is focused. The modulated reflected laser beam shoots on a photodetector with transimpedance and radio-frequency amplifiers, and then a modulated electrical signal is generated. After spectrum analysis, a signal with a particular frequency is generated. The signal synchronizes with the laser scan and forms an LVI image, overlapping with a normal optical image of the laser scanning area. Figure 2 is an example of an LVI image, showing the data and clock signals. Because LVI collects data in the frequency domain, it is necessary to map the transistor switching at a particular frequency. It is convenient to run the clock and data at different frequencies so that both the clock and data paths in the scan chain can be individually and simultaneously traced. Thus, it quickly became a powerful fault isolation technique for scan chain failures. With subsequent LVP, the defect for a scan chain failure can be narrowed down to an inverter or a node.

**IN-LINE SCAN CHAIN LOGIC MACRO DESCRIPTION**

The in-line scan chain logic macro can first be tested at metal-4 layer for early yield learning. It is comprised of several scan chains organized in 16 blocks. Each block has six packs, and each pack has six scan chains, which share the same clock buffer and preload data buffer (Fig. 3). Each scan chain group/block is composed of a different type of level-sensitive scan design and general scan

![Image](45x270 to 279x505)

![Image](113x64 to 472x209)
design latch. Most latches are representative of the ones used in product logic. The length of the scan chains/blocks varies according to the size of a given latch type. The smallest group of latches that can be tested independently is a pack, when all but one pack are skipped across all blocks with the help of a skip test scan chain. Between subsequent latches, a mux-2 circuit is implemented to enable two modes: serial scan, where data are fed from the previous latch, and preload mode, where data are preloaded from a buffer.

The in-line scan chain logic macro can be operated in three different modes: flush, scan, or preload. The first two modes are used to test the functionality of the macro. In the flush mode, all clocks are kept high, and serial data ripple through the latches from the scan input pins to the scan output pins. For the scan mode, the serial data are scanned through the latches by clocking the latches’ master and slave clocks.

The preload mode is used to electrically identify the failing latch in the event of a failure during the flush(scan mode operations, that is, when the data observed on the scan output pins do not match the expected data based on the pattern exercised on the scan input pins. In the preload mode, data are loaded simultaneously in all latches through the mux-2 circuit according to two possible sequences of 0101... or 1010..., respectively. These are referred to as checkerboard and reverse checkerboard patterns. As an example, in Fig. 4 the chain has a total of eight latches. The preloaded checkerboard pattern was “01010101,” and the observed scan-out pattern was “00000101.” After comparing these two patterns, the first suspected failing latch was found to be latch No. 5 from the scan-out pin. However, when the reverse checkerboard pattern “10101010” was preloaded, the observed scan-out pattern was “00000010.” It suggested that the first failing latch was latch No. 4 from the scan-out pin, and latch No. 4 with a stuck-at-0 fault also explained the observed scan-out pattern in the checkerboard preload test. With the checkerboard and reverse checkerboard tests, the first failing latch was identified to be latch No. 4 from the scan-out pin. In summary, the first failing latch is identified as the closest failing latch from the output pins of both complementary checkerboard and reverse checkerboard patterns.

The aforementioned latch callout identification procedure can be simplified with graphical display, which has been described in detail in Ref 14. Figure 5(a) shows an example of a single-latch failure, while Fig. 5(b) shows a clock-type failure. In Fig. 5, a white pixel indicates the measured data matches the expected data, while a dark pixel indicates the measured data do not match the expected data. The first datum scanning out from the scan chain is displayed at the extreme left. The first dark pixel counting from the left, whether in a checkerboard row or a reverse

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checkerboard row, pinpoints the latch callout (Fig. 5a). In Fig. 5(b), the six scan chains in a pack are failing at the same latch position, indicating a clock-type failure.

CASE STUDIES

Because the in-line scan chain logic macro is diagnosable and single-latch fallout can be identified based on the preload test, a hard single-latch failure may be successfully analyzed with routine physical failure analysis (PFA) using top-down scanning electron microscopy (SEM) inspection. However, as defined previously, the root cause of a clock-type failure could be any failure in the buffers and the interconnects of the preload data and clock lines, or a bridging fault in the preload data and clock input circuits in any individual latches. This involves a large area. Clearly, it is more challenging to perform PFA on a clock-type failure. Thus, for clock-type failures, LVI and LVP diagnoses are necessary for localizing the failure to a small area prior to PFA. In addition, for soft single-latch failures, although the possible defective area is the same as for hard single-latch failures, the defect causing a soft single-latch failure is much smaller and more subtle. Due to the subtle nature of the defect and the large number of transistors (as many as 50 per latch) that must be inspected, the success rate with routine PFA for soft single-latch failures is very low.

With the help of LVI and LVP, the success rate has been improved to approximately 85%. This section describes three cases that demonstrate how to apply LVI and LVP in diagnosing scan chain clock-type failures and soft single-latch failures. The root causes of these failures were found by subsequent PFA.

SKIP TEST SCAN CHAIN FAILURE

As previously mentioned, the in-line scan chain logic macro has been divided into 16 blocks, with different latch types or layout variations in each block. A skip test scan chain is implemented to enable each block to be tested individually. Before testing the 16 blocks of main scan chains, a skip test is performed to check the integrity of the skip test scan chain. In the first case study, a chip suffered from skip test failure. First, LVI was performed with the skip test scan chain under flush test, and the LVI image showed that the data could pass through the skip test scan chain successfully (Fig. 6a). However, the data signal stopped at the sixth latch, aligning with the last pack of block 1, when the skip test scan chain was run under clock mode test (Fig. 6b). This implied that the skip test scan chain failure was due to a clock signal issue. Both L clock and D clock signals were mapped with LVI, and it was found that the L clock signal propagation was fine, while the D clock

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signal propagation was broken (Fig. 7). Further comparison of the LVI signals from the clock buffers for blocks 1, 2, and 3 showed that many LVI signals were missing from the clock buffer for block 2, compared to those from the clock buffer for block 1, and no LVI signal came out from the clock buffer for block 3. This indicated that the D clock signal was supposed to propagate from the clock buffer for block 1, to the clock buffer for block 2, to the clock buffer for block 3, and so on; however, it stopped at the clock buffer for block 2. With layout tracing, it was found that there are several cascaded inverters for each clock buffer (Fig. 8). Laser voltage probing was employed to collect the waveform from each inverter. The waveforms shown at the right in Fig. 8 were collected from five points. Waveform 1 was from inverter 1, and waveforms 2 and 3 were from inverter 2 because of a long inverter. Waveforms 4 and 5 were from inverters 3 and 4, respectively. It clearly showed that the clock signal got stuck starting at inverter 3. The subsequent PFA showed a short between the source/drain contact and the gate contact at inverter 3, leading to a malfunction of this inverter, which was responsible for the skip test scan chain failure (Fig. 9).

**SCAN CHAIN CLOCK-TYPE FAILURE**

The second case study is a clock-type failure for a main scan chain pack, namely the same latch callout for

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all six scan chains in the same pack. These six latches are clocked by the same clock buffer and also are loaded by the same data buffer during preload mode (Fig. 10). The chip was subject to LVI analysis. The LVI image, shown in Fig. 11 with the clock signal in yellow and the data signal in blue, revealed that the data signal stopped at the latch callout. Figure 12 is a higher-magnification LVI image at the latch callout. It further showed that the clock signal is very weak in the latch callout. However, the clock signal in the clock buffer is still very strong. Furthermore, the latches close to the clock buffer have some data signal, while the latches far from the clock buffer do not have any data signal passing through. This implied that the signal became degraded between the clock buffer and the latch callout. Laser voltage probing was employed to check the clock signal in the latch callout (Fig. 13). Comparing the waveform from point 1 to the waveforms from points 2, 3, and 4, it was clearly seen that the waveforms at points 2, 3, and 4 were degraded. Based on layout tracing, the suspected defect was believed to be a highly resistant via in the interconnect from the clock buffer to the input of the latch callout. A subsequent focused ion beam (FIB) cross section on the suspected highly resistant via found a hollow V2 (Fig. 14).

**SCAN CHAIN SINGLE-LATCH SOFT FAILURE**

The third case study is a scan chain single-latch soft failure. The latch passed at high voltage but failed at low voltage. Although routine PFA on a scan chain single-latch hard failure can find a defect in most cases, a soft failure...
is usually caused by a very subtle defect that may be very
difficult to find. To maintain a high PFA success rate for soft
failures, fault isolation is often performed prior to destruc-
tive PFA. In this case, LVI and LVP were again employed for
the fault isolation. The LVI image of the clock signal and
the data signal for a reference scan chain, SO3, and the
failing scan chain, SO5, is shown in Fig. 15. It shows that
the clock signal (in yellow) appears to be acceptable in
both scan chains, while the data signal (in blue) stops at
the latch callout for SO5 and continues to propagate for
SO3. The higher-resolution LVI image (Fig. 16) from the
feeding latch and the latch callout showed that the data
actually had propagated to the master latch of the latch
callout but had not transferred to the slave latch. This
was further verified with LVP waveforms collected from
the master and slave latches, as shown at the right in Fig.
16. The subsequent PFA found a gate-to-source-resistant
short defect, which was responsible for the scan chain
single-latch soft failure.

**SUMMARY**

The unique capability of LVI to map periodic signal
propagation makes it very useful in scan chain diagno-
sis. For scan chain clock-type failures or single-latch soft
failures, routine PFA with top-down SEM inspection often
found no defect. Laser voltage imaging can clearly show
the broken point of the clock signal or data signal for
these failures. Follow-up LVP probing can further confirm
the failing nodes and help explain the failure signature.
Employing LVI and LVP in the diagnostic analysis greatly
improves the in-line scan chain logic macro failure analysis
success rate.

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