A SUMMARY OF THE ISTFA 2017 PANEL DISCUSSION:
STRIVING FOR 100% SUCCESS RATE

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During ISTFA 2017, we successfully hosted a Panel Discussion on the topic of “Striving for 100% Success Rate.” The failure analysis (FA) community knows that achieving 100% success rate is the ultimate goal for FA operations, and it holds particular importance for industries, such as automotive, aerospace, and oil companies, beyond the traditional semiconductor chipmakers. Five area experts among these industries shared their views on our panel regarding what “100% success rate” means to their organization, what challenges they encounter when working toward this goal, and the experiences they have in their daily work when operating toward this goal.

Dr. David Su, a director of the FA group at TSMC, Taiwan, began the Panel Discussion. David shared with the audience his belief that every sample is important, because finding the cause for failures is critical for fab process improvement. In the wafer fab foundry, a challenge can be the lack of sufficient product knowledge; therefore, it is particularly important to have strong partnerships with requesters in order to make the FA successful for root-cause finding. David emphasized the importance of a strong, experienced, expert team that is disciplined yet thinks outside the box and is fast but meticulous. He also cautioned that quickly finding a physical defect could lead to early, misguided satisfaction in the FA process, so be sure the analysis continues until the true root cause of the issue is found.

Our second presenter, Mr. Dan Bodoh, a technical director in the Product Diagnostic Center at NXP, focused mainly on electrical FA and fault isolation for new product introduction (NPI). Dan indicated the importance of having a definition of “failure analysis success.” NXP uses three criteria for successful FA: (1) conclusive evidence that connects electrical behaviors to a physical defect, or (2) a fingerprint or a signature is already agreed upon, or (3), for early NPI debug, significant contribution to the product and design team’s understanding of an issue. Dan shared the belief that FA leadership has a responsibility to keep an eye on the processes in the lab, because it is okay to make a mistake, but patterns of mistakes must be investigated, as it is critical to learn from them. He also encouraged holding “challenging analysis meetings” to brainstorm with the team, and building a team led by experienced people not bound by the daily cycle-time pressure but empowered to help the team have better productivity and quality daily analysis work.

Unlike the first two speakers from the traditional semiconductor wafer fab and chipmakers, our next three invited speakers were from companies in special application areas.

Dr. Oliver Senftleben, a senior technical expert from Audi Semiconductor Lab in Germany, shined light on the automakers’ perspective of 100% FA success rate. For automakers, 100% success rate is a requirement, not a strategic goal. On average, there are 6000 to 8000 semiconductors in each car; therefore, a 1 ppm random failure rate means 10,000 to 15,000 defects in car components, based on yearly production volume for Audi. A 100% success rate is imperative for qualification failures, because findings impact new vehicle project releases. A typical qualification sample size is six devices; thus, failures could likely imply systematic issues. Rapid determination of countermeasures, even based just on the failure symptoms, is critical for 0 km failures, because potential systematic failures are pushed into the field every 80 s per production line. Quick root-cause identification of field failures is a priority, because systematic and epidemic failures lead to high warranty costs and
harm the overall brand image. An automotive industry challenge is the time-consuming communication V-model, where field failure information passes down through multiple supply chain tiers to the semiconductor supplier, and then the semiconductor supplier’s findings pass up through the same channels to the original equipment manufacturer (OEM). To achieve more visibility, better results, and quick feedback to the OEM, automakers are joining forces with the semiconductor chipmakers to analyze high-priority failures. Quick identification, communication, and prioritization of systematic and epidemic failures within the random failure baseline is a major challenge within the entire supply chain.

After hearing how critical high success rate is to the automaker, the Panel Discussion moved on to another highly challenging area, aerospace applications. Mr. Ryan Ross, a technical supervisor from NASA’s Jet Propulsion Laboratory in Pasadena, Calif., declared that the aerospace application is extremely failure adverse. A high success rate for FA is essential to ensure the safety and reliability of future missions. The components used in aerospace applications are generally custom-made in low volume and with extreme reliability requirements. All possible issues must be uncovered and corrected during development phases, because there are not yet field returns from Mars. Ryan emphasized the importance of “tiger teams,” where analysis experts, including a lead investigator, component specialist, FA engineers, and subject matter experts, gather in one room to work through issues. This good team work and broad knowledge base, along with strictly following process flows, improves the success rate and preserves the integrity of aerospace industry investigations.

After looking up to the sky, we finalized our Panel Discussion with a look at what 100% success rate means to the oil industry. Mr. John Bescup, an electrical engineer with Weatherford in Houston, Texas, spoke about electronic devices used for “logging while drilling” that collect useful real-time data to assist the drilling engineers in finding oil reservoirs. The printed circuit boards and components used must meet high reliability standards and function at high-temperature conditions in harsh vibration environments. Failures on electronic components can cause costly downtime during the drilling operation, so a high success rate on FA is vital for the success of drilling service companies in the oil industry. Commonly seen failures are often related to package issues exacerbated by the harsh underground environment, so a broad knowledge base of metallurgy, chemistry, mechanical engineering, and electrical engineering is vital for FA success.

Throughout the Panel Discussion, the audience engaged with each panelist by asking numerous questions, and the discussion was a pronounced learning opportunity for those involved. We all are striving toward 100% success rate in our daily lives, and this Panel Discussion provided a little more knowledge and advice on how we can achieve it.

**ISTFA 2017 FOCUSED ION BEAM (FIB) USER GROUP**

Moderators: Steven Herschbein, GLOBALFOUNDRIES, and Michael Wong, FEI/Thermo Fisher Scientific

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This year we had six presentations that covered a wide range of topics, including:

- Three papers that featured alternate (non-gallium) ion beams
- A methodology for evaluating the relative merits of competing FIB platforms
- A guide for deciding which backside edit sample-preparation method to select
- Planar FIB deprocessing from the backside and frontside
- A sub-pico-amp FinFET edit example using the latest gallium circuit edit platform

The session’s first speaker was Adam Steele from the startup zeroK NanoTech, working in conjunction with the National Institute of Standards and Technology on the subject “Next-Gen FIB and SIMS with Low-Temperature Ion Source FIB Platform.” Adam introduced the LoTIS (successor to the earlier MOTIS), featuring Cs+ as a low-temperature ion source. By mounting the new column on a Vectra platform, they retained the full gas-delivery system (commonly used etch and deposition gases) and other desirable system features.

Key advantages of Cs+ LoTIS is its small spot size yet high beam current density availability at low beam energy, reduced implant depth, and greatly reduced straggle.
Demonstrated tests included 1.8 nm resolution at 10 kV/1 pA, low invasiveness in a chip edit simulation, excellent imaging and nanomachining control, and ultrafast secondary ion mass spectrometry (SIMS) acquisition.

Sharang, from Tescan Orsay, presented the second talk, “Delayering Capabilities Using Xe+ Plasma FIB and Associated In-Situ Nanoprobing Operations.” He began by showing impressive delayering results from the M4 metal layer down to gates over a 40 × 40 µm area on a popular 14 nm FinFET processor product. The resulting surface roughness, as measured by atomic force microscopy technology, was very low, which enabled easy in situ nanoprobing at the individual FinFET transistor level. Results were shown from an eight-tip stage-mounted prober assembly and even an in situ atomic force probe.

However, being able to plasma-FIB deprocess the upper levels (thick, wide, and not necessarily fully planarized) would normally require starting with highly inexact mechanical parallel polishing. The trick shown was to begin the process on flip-chip module-mounted dice, as though it was the start of an FIB chip edit. Sharang began with ultrathin CNC contour milling followed by XeF₂ clearing of all remaining silicon to the underside of the fin mandrel and shallow trench isolation regions. Planar deprocessing then proceeded, using a proprietary gas and Xe⁺ beam process through the thin lower interconnects and into the thicker layers from the bottom side upward.

Michael DiBattista from Varioscale presented “A Decision Tree for FIB Sample-Preparation Strategy.” The idea for this talk came from a lunchtime discussion some months ago about all the possible options available to those engaged in FIB chip circuit edit. Depending on the tools at one’s disposal, time issues, edit-site peculiarities or the need to do multiple edits, and customer requirements (system use or test with or without probing), one may have either a clear choice or multiple possible paths. These include, but are not limited to, localized or wide-area partial or full-thickness silicon trenching (laser chemical etching, plasma FIB, or FIB XeF₂) or mechanical prethinning (localized pocket, moderate thickness remaining with or without contour following, or ultrathin silicon remaining). The need for good end-pointing and various methods were explored. From the “nuclear option” to ultrathinning, Mike stepped through each scenario and suggested the best toolset to use to achieve individual sample-prep needs.

Valery Ray of PBS&T, MEO Engineering/University of Connecticut, presented the fourth paper, “Quantifiable Comparative Evaluation of FIB/SEM Instruments.” Valery discussed the need to design quantifiable evaluation tests for FIB systems, noting that “canned” demos are designed to exploit the best features of a given tool but not necessarily show the full picture of the tool. He showed examples of standardized samples and a number of qualification tests, including beam burns, current versus dose, drift tests, patterning performance tests, and imaging tests. He also suggested some customized combination tests that will emulate specific-use cases. Being prepared with one’s own evaluation suite that can be performed on all FIB platforms under consideration will help end-users make the best tool-purchasing decision.

The fifth paper, “Sub-Pico-Amp Focused Ion Beam (FIB) for Circuit Edit on FinFET Technology,” was given by Hideo Tanaka from FEI/Thermo Fisher Scientific. Hideo’s talk explored the challenges that are arising from shrinking process nodes that accompany the adoption of FinFET technology. He stressed that a circuit edit solution which includes sub-pA beam currents, precision milling, and optimized gas and recipes must be precise. Critical for meeting today’s chip edit challenges is an improved secondary-electron detector to be able to image the scant amount of signal for end-pointing and so on. He showed a case study of circuit edit work with emphasis on the key elements required to enable a successful, functional modification.

The sixth and final paper of the workshop session, “Neon GFIS-Induced Chemical-Assisted Etch and Beam-Induced Deposition Characterization,” was presented by Rick Livengood of Intel. The first part of Rick’s talk included a review of neon gas field ion source (GFIS) technology and how it has been used for nanopatterning, surface analysis, transmission electron microscopy prep, and early circuit edit attempts. He noted that some of the key attributes to GFIS technology are that neon generates two to three times the secondary electron yield relative to gallium, and also, the sputter yield is half of gallium. That provides more reaction time along with better visual and instrumentation end-pointing.

The second segment included an update of recent experimental results comparing neon via sputtering versus gas-assisted neon etching, and deposition of oxides and metals using neon as the primary beam. Much of the work was done using a new gas system from Xidex that features dual opposing XeF₂ gas nozzles along with nozzles for an oxide source (PMCTS and oxygen). Overall, neon appears to address some of the limitations presented by gallium for chip edit and will be a good complement as a dual-column system for use on sub-10-nm process nodes.
In a marked change from previous ISTFA events, the FIB User Group meeting was held concurrently with the Contactless and Nanoprobing User Group during the two-hour lunch break on Thursday, November 9. Despite some concern, the “lunch and learn” experiment seemed to work. Overall attendance was up from last year, and audience participation was strong after each paper and during the panel discussion at the end. A peak attendance of 97 was recorded just before 1 p.m. The organizers also wish to thank Thermo Fisher Scientific for their sponsorship of the event.

ISTFA 2017 CONTACTLESS OPTICAL/NANOPROBING EFA USER GROUP

Moderators: Dan Bockelman, Intel Corp.; Sweta Pendyala, GLOBALFOUNDRIES; and Nebojsa Jankovic, NXP Semiconductors
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Dr. Daminda Dahanayaka (GLOBALFOUNDRIES, Essex Junction, Vt.) gave the first presentation, “Challenges of FEOL Sample Preparation for Nanoprobing of Advanced Nodes.” The goals in sample prep are good edge definition of conductors, protection of underlying structures, and good surface electrical conductivity for probe contacting. Because scaling reduces line widths as well as film thicknesses, specialized sample preparations for both scanning electron microscopy (SEM) and atomic force microscopy (AFM)-based probers are required. First, the IC is delayered down to the layer of interest. Next, topographical relief of the contacts is performed 2 nm below the surface with a diamond slurry. Colloid slurry relief is not sufficient for AFM probers but is sufficient for SEM nanoprobing. An alternative to diamond slurry is HF reactive ion etch (CF₄, CHF₃, CH₂F₂, etc.). The HF yields poor images, and CF₄ etches SiN faster than SiO₂, but C-F leaves polymer deposits. Finally, a third alternative is ion milling (argon, N₂, O₂). The N₂ etches a little faster than argon or O₂. Overall, this presentation emphasized how important sample prep has become as devices have continued to scale aggressively.

The second presentation, “Recent Advances in Nanoprobing,” was given by Dr. Martin Von Hartman (Intel, Hillsboro, Ore.). The presentation discussed nPIII upgrades compared with the nPII system. The xProber using the Zeiss SEM is the precursor to the nPIII, which uses a substage. Faster nanoprobing is needed, especially for future technologies. Intel has seen increased demand for nanoprobing year after year, which is more than was anticipated. Essential capabilities of a nanoprober are minimal drift; maximum time on contact; SEM image quality; quality probe tips; good sample prep; automation; capability to detect opens, shorts, resistive shorts, and so on; and minimal e-beam invasiveness. Primary benefits of the nPIII system are 50% reduced beam current from nPII, a lower working distance of less than 4 mm, and greater than 10 min time on contact. Pulse probing was aimed at finding resistive gate failures, but it is too slow and not done routinely in the Intel labs. There is need for an alternating current test to investigate gate resistance, but it must be fast. It can take hours to set up for pulse probing.

The third presentation, “Advantages of Electrical Optical Voltage Probing (EOP) Using a Digitizer,” was given by Brett Adler (Hamamatsu, San Jose, Calif.). Sampling long-duration test loops enables detectability of timing behavior not possible with an oscilloscope. The technique uses a continuous-wave laser. Carrier concentrations under the transistor gate result in reflection changes as the transistor switches, and the changes are felt in the reflected beam. The reflected beam is sampled through the use of a detector, and the waveform information is derived. It allows zooming into any fast glitch in a waveform. The EOP mapping combined with a digitizer works well for SRAMs. These enable new analysis with 31.25 ps resolution. The technique uses up to four Giga-samples per second, and 500,000 points can be sampled at 250 ps resolution.

The fourth presentation, “Fault Localization—LTP Technique Using High-Speed Digitizer versus Oscilloscope,” was presented by Dr. Mike Bruce (Semicaps). Laser timing probe (LTP) measurements have been limited by the acquisition speed of oscilloscopes. Three spectrum analyzers have been used in parallel, due to the triggers in short test loops.
This is overcome with a high-speed digitizer capturing all the triggers for a short-loop acquisition time improvement of more than 50×, even up to 500× faster than a LeCroy oscilloscope. A 2 GHz bandwidth digitizer is 12 bits. For slow loops, high-bandwidth oscilloscopes are noisy. The digitizer allows for logic analysis in real-time, and binary searches are supported.

The fifth presentation, “Visible versus IR for Laser Probing,” was given by Neel Leslie (Thermo Fisher Scientific, Fremont, Calif.). Laser voltage probing and laser voltage imaging directly expose electrical functionality of an IC or cell. The interplay between optical spatial resolution (inversely proportional to wavelength) and transmission through the silicon has necessitated near-infrared wavelengths (1064 to 1340 nm). Visible light probing has shown improved resolution (1320 to 785 nm, resolution improves 40%); however, trade-offs exist with laser invasiveness and silicon thinning. To use the technique, silicon must be thinned below 10 µm. However, the impact of laser invasiveness on the measurements is still a question, but it can be reduced by lower laser power, less than 2 mW. At 5 µm silicon thickness, the transmission is 60%.

The final presentation, “Techniques for Successful Backend-of-Line Nanoprobing,” was given by Weston Hearne (Thermo Fisher Scientific, Richardson, Texas). Electron beam induced resistance change (EBIRCH) and electron beam absorbed current (EBAC) for back-end-of-line (BEOL) fault localization have become significant use cases for nanoprobing. Fifty percent of nanoprobing is for BEOL EBAC/EBIRCH, but frontside EBAC/EBIRCH accounts for 90% and backside EBAC/EBIRCH for 10%. With EBAC, nets remain intact.

This year the Contactless Fault Isolation and Nanoprobing User Groups were combined into a single User Group meeting. The User Group had six presentations focusing on topics in both contactless optical probing and nanoprobing areas. All presentations were well received, with follow-on discussions and questions and answers during and after each presentation. Each of the presentations showcased innovations in the contactless probing and nanoprobing areas and showed how the industry is moving forward to meet the challenges of semiconductor failure analysis today. More than 50 people attended the User Group meeting, and we look forward to a great 2018 User Group meeting as well. The organizers wish to thank Semicaps for their sponsorship of the session.

ISTFA 2017 SAMPLE-PREP/3-D PACKAGE-PREP USER GROUP

Moderators: Nathan Bakken, Intel Corp., and Tim Hazeldine, ULTRA TEC
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The Sample-Prep User Group, sponsored by Varioscale, Inc., hosted four technical presentations toward the development of new capabilities in the laboratory. The first presentation discussed ultra-flat repackaging as an alternative strategy to address the increasing complexity of coefficient of thermal expansion mismatch and other packaging-induced strains. The next two presentations addressed case studies where alternative deprocessing techniques were successful for particular current and proposed applications. The final presentation reviewed workflows to assemble or reassemble multiple chip packages to enable physical debug workflows. The session was concluded by an interactive discussion where the audience engaged to publish an answer to the question: “What are the greatest challenges facing 3-D IC package and sample-preparation technologists until 2022?”

“Rapid Repackaging of Die for Backside Physical Failure Analysis” was presented by Scott Silverman of Varioscale, Inc. The presentation noted the benefits of backside silicon deprocessing methodology that are becoming increasingly threatened by a packaging roadmap that continues to include thinner and less rigid substrate materials. In addition to more complex shapes caused by the package roadmap, the requirement for thinner silicon found in Z-height constrained applications or to reduce backside absorption also benefits from highly planar samples. A video was provided to show the implementation of an electrically or optically initiated foil soldering solution that has been successful in preventing thermal damage and was used to achieve surface flatness after mounting in the sub-100-nm range for an ~8 mm × 8 mm die. Also discussed was the selection of carrier materials to potentially
include depleted uranium in cases where ultimate stiffness is desired. The question-and-answer session addressed the minimum machining radii achievable for pocket mounting using milling tools, and an extension below 50 µm radii enabled with laser machining techniques.

“Thin, Smooth, and Curvy—The Confessions of a Sample-Prep Specialist” was presented by Jim Colvin of FA Instruments, Inc. Jim addressed the need for increasingly controlled sample preparation across complex devices that is driven both by new failure analysis methodologies as well as increased tolerances for other testing requirements. He reviewed selected cases where successful processes occurred. Data showing the “orange-peel” effect as a function of temperature were reviewed, and it was demonstrated that mitigation could occur as the temperature was increased from 20 to 80 °C within the detection limits of backside optical microscope inspection. The orange-peel effect was interpreted as the residual Z-strain resulting from the C4 attach process, which is particularly easily observed when remaining silicon thickness is below 5 µm. Some applications for capacitive and resistive endpointing mechanisms were highlighted, and the potential direction for in situ “probing while sample preparing” methodology was also shared. The audience initiated some discussion on the observable-by-eye color change that occurs when silicon is thinned to single-digit remaining thickness, with disagreement as to whether this observation could lead to development of simpler thickness metrology methodologies.

“Effective Microwave-Induced Plasma Decapsulation for Advanced IC Packages” was presented by Erik Jordan of Nisene Technology Group. The discussion focused on limitations due to extended throughput time or incompatibility with emerging materials systems facing traditional reactive ion etching processes. Also presented was the potential for application of microwave-induced plasma deprocessing to include oxygen, argon, carbon tetrafluoride, or other process gases as a solution to the decapsulation requirements roadmap. Examples from copper/palladium bonds that are highly reactive to wet deprocessing were reviewed in addition to examples demonstrating the deprocessing workflows for emerging silver bonding materials systems.

“Wire Bond Connected High-Bandwidth Memory Attach on 3-D Stacked Die for Physical Debug Sample Prep” was presented by Nathan Bakken on behalf of Charles Ladwig, both of Intel Corporation. Heterogeneous integration of multiple dice at the package level was shown to be an increasingly common and threatening trend for physical debug techniques that traditionally rely on direct access to the backside silicon substrate. When dice are stacked or keep-out-zones required for physical debug techniques are otherwise infringed upon, it was proposed that an opportunity to reassemble die components in an orientation or workflow order suitable for debug could be pursued. Case studies were reviewed, including die reattach post-circuit-edit workflow as well as direct-to-die attach of LPDDR4 to enable optical probing of the base die in a package-on-package configuration where access to memory channels was a requirement for the fault isolation workflow.

Following the presenter topics, the moderators enabled a round-robin discussion of the five-year challenges forecasted for the sample-prep and 3-D package community. The audience participated by alternating between descriptions of future challenges and the relative magnitude of these challenges, with results tabulated and debated in real-time. As a result of a few dozen inputs from a variety of industry experts, seven challenges were identified for sample-prep and 3-D packaging technologists over the next five years:

- Absence of a roadmap consortium
- Proliferation of manufacturable processes out of the research and development lab
- Reduction of the quantity of and artistry required for process steps
- Attracting the next generation of engineering talent
- Getting support from design-for-test partners
- Reducing invasiveness
- Enabling budgets

The session successfully generated discussion and knowledge-sharing for over 75 people in attendance.